AMENDMENTS TO THE CLAIMS

Please amend claim 1 and add claims 7-9 as follows. This listing of claims replaces all previous versions and listings of claims.

1. (Currently Amended) A context based direct memory access architecture, comprising:

a memory;

a plurality of ports, wherein each port has an associated buffer located at and dedicated to the port for temporarily storing data transferred through the port, and wherein each port has an associated direct memory access channel for accessing the memory;

a direct memory access controller that receives requests for accessing the memory by the plurality of ports, wherein each request is received from one of the plurality of ports, and wherein the direct memory access controller stores parameters defining the direct memory access operations for each port, and wherein after a request is received from a port, the direct memory access controller loads registers used by the direct memory access controller with the parameters for a direct memory access operation, in response to the request from the port and independent of any instructions from a host central processing unit, to enable the port to access the memory and transfer data between the memory and the buffer associated with the port.

2. (Previously Presented) The context based direct memory architecture of claim 1, further comprising a central parameter store for storing parameters for each of a plurality of DMA channels corresponding to each of the plurality of ports.

3. (Previously Presented) The context based direct memory architecture of claim 2, wherein the direct memory access controller further comprises means for servicing the request, comprising:

means for queuing a memory operation;

means for updating parameters; and

means for fetching and storing parameters in the central parameter store.

4-6. Cancelled.

7. (New) A direct memory access controller for context based direct memory access architecture, that receives requests for accessing a memory by a plurality of ports; wherein each port has an associated buffer located at and dedicated to the port for temporarily storing data transferred through the port and has an associated direct memory access channel for accessing the memory; wherein each request is received from one of the plurality of ports; wherein the direct memory access controller stores parameters defining the direct memory access operations for each port; and wherein after a request is received from a port, the direct memory access controller loads registers used by the direct memory access controller with the parameters for a direct memory access operation, in response to the request from the port and independent of any instructions from a host central processing unit, to enable the port to access the memory and transfer data between the memory and the buffer associated with the port.

8. (New) The direct memory access controller of claim 7, further comprising a central parameter store for storing parameters for each of a plurality of DMA channels corresponding to each of the plurality of ports.

9. (New) The direct memory access controller of claim 8, further comprising a means for servicing the request, comprising:

means for queuing a memory operation;

means for updating parameters; and

means for fetching and storing parameters in the central parameter store.